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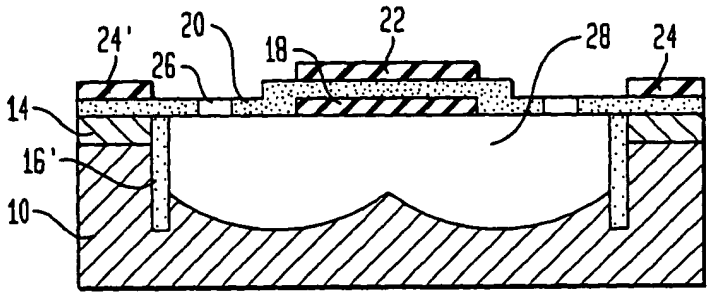
(54) Thin film resonators fabricated on membranes created by front side releasing

(57) A new bulk resonator may be fabricated by a process that is readily incorporated in the traditional fabrication techniques used in the fabrication of monolithic integrated circuits on a wafer. The resonator is decoupled from the wafer by a cavity etched under the resonator using selective etching through front openings (vias) in a resonator membrane. In a typical structure the resonator is formed over a silicon wafer by first forming a first electrode, coating a piezoelectric layer over both the electrode and the wafer surface and forming a second electrode opposite the first on the surface of the piezoelectric layer. After this structure is complete, a number of vias are etched in the piezoelectric layer exposing the surface under the piezoelectric layer to a selective etching process that selectively attacks the surface below the piezoelectric layer creating a cavity under the resonator.

FIG. 8



EP 1 180 494 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention:

[0001] This invention relates to electrical bulk resonators and more particularly to a method for manufacturing a thin film resonator on a membrane over a cavity on a semiconductor substrate as part of a monolithic integrated circuit.

2. Description of Related Art:

[0002] In the design of radio receivers, particularly paging receivers, cellular radios, and microwave satellite communication systems, it is desirable for components which form the system to take up as little space as possible. It is desirable for as many components as possible to be integrated into a single integrated circuit in the form of monolithic circuits.

[0003] A monolithic integrated system, requires less space, is more reliable, has a lower power consumption, has more precise temperature control, and has a higher shock tolerance, than one which requires multiple independent components. It is also easier to produce matched resonator and oscillator circuits when they are produced on the same substrate, and, typically monolithic structures present lower manufacturing costs at every stage of design and production. Thus the advantages of monolithic integration are numerous.

[0004] An important element used in the type of equipment mentioned above is an electronic filter. The present state of the art employs resonant electromechanical structures in designing such filters. The structures and materials used depend on the frequencies of the signals involved, and can be separated into three major categories, (a) mechanical, (b) quartz crystals and (c) piezoelectric materials.

[0005] The later are particularly useful for frequencies above about 300 Mhz where a thin film non-conductive piezoelectric resonator is commonly used. Such resonators may be one of two basic types, a surface acoustic resonator (SAW) or a bulk acoustic resonator (BAW). SAW resonators don't respond well at frequencies above 2GHz, and are not able to handle radio frequency (RF) signals at high power.

[0006] BAW resonators on the other hand, do not suffer such limitations. BAW resonators in their basic form comprise a piezoelectric material sandwiched between two opposing electrodes. Such resonators, however, in order to perform with the required efficiency require an unsupported structure, which means that when such resonators are used as a part of an integrated circuit structure, such as a CMOS, they should be placed either over a cavity in the semiconductor support, or should be elevated therefrom. In addition such BAW resonators, in order to be commercially useful, should be able to be manufactured as part of the normal CMOS and Bipolar silicon processing techniques.

[0007] The art has both recognized the advantages of a monolithic BAW resonator and the need to build such resonator as an unsupported structure. A solution to this design problem is proposed in United States patent number 5,260,596, issued November 9, 1993 to Dunn et al.

[0008] According to Dunn et al. unsupported mechanical, quartz and piezoelectric electromechanical resonators may be constructed on a support such as a silicon semiconductor wafer, by first micro-machining a cavity in the substrate and filling the cavity with a sacrificial non silicon filler such as a phosphorous silicate glass (PSG). The resonator is next built on the sacrificial filler and extends beyond the cavity limits to the substrate surface. The filler provides support during the manufacturing steps. Once the resonator structure is completed the sacrificial filler is removed by etching. The result is a BAW resonator that is constructed over a cavity and is, therefore substantially unsupported.

[0009] While the disclosed resonator offers advantages over prior resonators, the ' method of its fabrication, which requires first creating the cavity, then filling and finally etching the filler away from under the resonator itself, is not a method that can be readily incorporated in the traditional fabrication techniques used in the fabrication of monolithic integrated circuits. Further more, the etching process to remove the filler material disclosed in the prior art is a liquid etching process which also attacks aluminum and which sometimes washes away small parts of the circuit.

[0010] Clearly there is still a need for a resonator which can be monolithically integrated with other semiconductor devices, in which the bulk structure resonator is not in contact with anything which would inhibit vibration-However, there is also as clearly a need for a method to fabricate this resonator which can be readily integrated in the typical monolithic integrated circuit manufacturing processes and which is less harsh on the materials used to construct the resonator.

[0011] It is, therefore, an object of the present invention to provide a method and resulting resonator whose manufacturing steps may be readily integrated in a typical CMOS or Bipolar Silicon processing or added to such process as a post process step.

SUMMARY OF THE INVENTION

[0012] The above object is obtained in accordance with this invention through a new bulk resonator incorporated in the traditional fabrication techniques used in the fabrication of monolithic integrated circuits on a wafer. The resonator is decoupled from the wafer by a cavity etched under the resonator using selective etching through front openings (vias) in a resonator membrane.

[0013] As an example, the resonator may be a bulk type resonator, fabricated on a semiconductor wafer

support preferably using a piezoelectric material, having the following structure:

(a) A semiconductor wafer support.
(b) A cavity extending through the surface of the wafer partially into the support body;
(c) a piezoelectric membrane extending over the support and the cavity. The membrane has an area over the cavity, an underside facing the support surface and a topside opposite the underside.
(d) A first electrode is adhered to the piezoelectric membrane underside over a portion of the membrane area over that extends over the cavity.
(e) There is a second electrode on the topside of the piezoelectric membrane over the first electrode and substantially coextensive with it.
(f) There is also at least one via in the piezoelectric membrane adjacent the first and second electrodes.

[0014] Preferably there is also a isolation layer between the wafer surface and the underside of the piezoelectric membrane, and the cavity is formed at least in the isolation layer. The isolation layer may be a high resistivity layer.

[0015] Such structure may be fabricated to generate a bulk resonator structure on a wafer by a method comprising the steps of:

(A) forming a isolation layer on an upper surface of the wafer;
(B) depositing over the isolation layer a first conductive layer and patterning the first conductive layer to form a first electrode;
(C) depositing over the isolation layer and first electrode a piezoelectric layer;
(D) forming a second electrode over the piezoelectric layer and over the first electrode;
(E) opening at least one via through the piezoelectric layer along at least one side of the first electrode and spaced therefrom; and
(F) using a dry etching process to form a cavity under the first electrode and adjacent piezoelectric layer by etching away at least a portion of the isolation layer under the first electrode and adjacent portions of piezoelectric layer by introducing an etchant through the via, selected to etch the isolation layer and to not significantly attack the piezoelectric layer and the electrodes .

[0016] Typically, in step (C), a plurality of vias are opened, surrounding the first electrode and the dry etching step is a gaseous etch process. When the wafer is a silicon semiconductor wafer and the isolation layer is a sputtered silicon layer deposited over the wafer surface, the etching step preferably uses xenon difluoride (XeF_2).

[0017] Using the above method, one may fabricate during the normal manufacturing steps common in the fabrication of monolithic circuits a bulk acoustic resonator on a silicon wafer, with electrodes made of Al, and a AlN piezoelectric membrane. The membrane is self supporting and extends completely over a cavity etched under the electrodes in the supporting wafer. The membrane is isolated from the silicon semiconductor wafer surface by a high resistivity sputtered silicon layer deposited between the membrane undersurface and the silicon support surface, and includes a plurality of vias extending therethrough located adjacent to and around said electrodes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The invention can be more fully understood from the following description thereof in connection with the accompanying drawings described as follows.

[0019] Figure 1 shows in schematic elevation a portion of a wafer on which there is to be constructed a BAW resonator following a first step of a process to manufacture such resonator in accordance with this invention.

[0020] Figure 2 shows in schematic elevation the same portion of the wafer shown in figure 1 following a second step of the process to manufacture such resonator in accordance with this invention.

[0021] Figure 3 shows in schematic elevation the same portion of the wafer shown in figure 2 following a third step of the process to manufacture such resonator in accordance with this invention.

[0022] Figure 4 shows in schematic elevation the same portion of the wafer shown in figure 3 following a fourth step of the process to manufacture such resonator in accordance with this invention.

[0023] Figure 5 shows in schematic elevation the same portion of the wafer shown in figure 4 following a fifth step of the process to manufacture such resonator in accordance with this invention.

[0024] Figure 6 shows in schematic elevation the same portion of the wafer shown in figure 5 following a sixth step of the process to manufacture such resonator in accordance with this invention.

[0025] Figure 7 shows in schematic elevation the same portion of the wafer shown in figure 6 following a seventh step of the process to manufacture such resonator in accordance with this invention.

[0026] Figure 8 shows in schematic elevation the same portion of the wafer with the resonator structure completed.

[0027] Figure 9 is a schematic top view of the resonator structure depicted in figure 8.

[0028] Figure 10 shows in schematic elevation a wafer portion prepared for use in fabricating a resonator according with an alternate embodiment of this invention.

[0029] Figure 11 shows in schematic elevation the same portion of the wafer shown in figure 10 following a second step of the process used to manufacture the

alternate embodiment of the invention.

[0030] Figure 12 shows in schematic elevation the same portion of the wafer shown in figure 11 with the alternate embodiment of the resonator completed.

DESCRIPTION OF THE PREFERRED EMBODIMENT (S)

[0031] Throughout the following detailed description, similar reference characters refer to similar elements in all figures of the drawings. The drawings are illustrative only and are used in order to explain, rather than limit the invention.

[0032] Referring now to figure 1, there is shown a portion of a semiconductor support 10 which is preferably a silicon wafer. On a surface 12 of the wafer there is, preferably, deposited using conventional technology such as sputtering, an optional silicon layer to form a isolation layer 14. Preferably this layer is between about $2*10^{-6}$ and $5*10^{-6}$ meters thick.

[0033] A trench 16 (or a series of trenches) is next etched through the isolation layer 14 and into the silicon wafer delineating a desired area 17 as better shown in figures 2 and 9. Etching of the trenches is preferably done using the well known Reactive Ion Etching technology, (RIE). The trenches are next filled with low temperature oxide (LTO), to produce an etch delimiting barrier 16' which is used in later step to contain the etching of the wafer and isolation layer to within the area within the desired area 17.

[0034] A conductive layer such as aluminum is next deposited to a typical thickness of between about $0.2*10^{-6}$ and $0.3*10^{-6}$ meters over the isolation layer and patterned (masked and etched according to a desired pattern using photolithography) to form a first electrode 18 on the surface of the isolation layer within the desired area 17, as shown in figure 4. Once the first electrode has been created, there is deposited over the surface of the isolation layer and over the first electrode 18, a layer 20 of a piezoelectric material such as a layer of AlN. The piezoelectric AlN layer is deposited to a thickness of about $1*10^{-6}$ and $5*10^{-6}$ meters, preferably $2.7*10^{-6}$ meters. However the thickness of the piezoelectric material may be different depending on the design frequency response of the resonator.

[0035] A second conductive layer, again preferably an aluminum layer is deposited over the piezoelectric layer and patterned to form a second electrode 22 substantially coextensive and over the first electrode 18, as shown in figure 7. At the same time connector or bond pads 24 and optionally 24' are formed also over the piezoelectric material, preferably outside the desired area 17 delimited by the trenches filled with LTO. These pads are connected to the second electrode through a conductive path 23 and 23' respectively, which is also preferably formed by photolithographic patterning simultaneously with the second electrode and bond pads. The bond pads serve as external connection points for accessing the resonator.

[0036] Both the electrodes, conductive paths, bonding pads and the piezoelectric layer are preferably deposited using physical vapor deposition or sputtering. Depending on the desired resonant characteristics of the BAW resonator, the size of the electrodes will vary. Typical dimensions for a square shaped electrode pair are between $100*10^{-6}$ and $400*10^{-6}$ meters for the sides.

[0037] Once the second electrode has been formed, a number of vias 26 are formed, preferably by etching, through the piezoelectric material within the desired area 17. The vias are placed adjacent the electrodes and preferably evenly spaced all around the electrodes. Typical via diameters are between $5*10^{-6}$ and $20*10^{-6}$ meters, preferably about $10*10^{-6}$ meters and extend through the piezoelectric layer to the surface of the isolation layer 14.

[0038] The next step, illustrated in figure 8, is the etching of a cavity 28 under the first and second electrodes so as to isolate from the support 10 the bulk resonator formed by the three layer combination of the first electrode 18, piezoelectric layer 20 and second electrode 22. This is accomplished in a dry etching process by introducing through the vias 26 an etchant, which is preferably a gaseous etchant that attacks the isolation layer and may also attack the underlying support, but does not attack the piezoelectric material or the electrodes. In a preferred resonator structure, a bulk acoustic resonator is formed using aluminum as the conductive material for the first and second electrodes and aluminum nitride (AlN) for the piezoelectric material. The support is a silicon wafer and the isolation layer is a high resistivity layer such as a silicon layer between the piezoelectric layer and the wafer surface. The etchant used is XeF_2 gas which attacks the silicon but does not attack the aluminum, the AlN or the LTO barriers. Thus introduction of the XeF_2 etches away an area beneath the AlN layer to form a cavity 28 leaving an AlN membrane extending over the cavity to the surface of the isolation layer on the supporting wafer having an unsupported area that includes the BAW resonator over the etched cavity. The cavity 28 may or may not extend all the way through the isolation layer. Typically the cavity depth is from about $2*10^{-6}$ meters to about $10*10^{-6}$ meters. Electrical connections to the bonding pads complete the resonator.

[0039] In a variation of the above process illustrated in part by figures 10, 11 and 12, the cavity 28' size may be designed fairly accurately by starting with a wafer 10' that already includes a bottom etch barrier 30. In the example given above where the support is a silicon wafer, such barrier may be created by first growing or depositing a SiO_2 layer 30 over the silicon wafer surface. The isolation layer 14, again typically a high resistivity Silicon layer, is next deposited over the SiO_2 layer, again preferably using sputtering.

[0040] Such wafer structure has a SiO_2 layer 30 sub-

stantially parallel with its surface, as shown in the figures. The remainder of the manufacturing process is the same as previously described with the barrier trenches 17 extending at least to the SiO_2 layer. The SiO_2 layer may be thermally grown or deposited (LTO). In this manner, as the SiO_2 layer is also not attacked by the XeF_2 gas, the portion of the support enclosed on top by the piezoelectric layer 20, and the first electrode 18, along the sides by the LTO filled trenches 17'and on the bottom by the SiO_2 layer 30 is etched away completely leaving behind a BAW resonator over a well defined cavity 28' as shown in figure 12.

[0041] The end result of the above process is a BAW resonator structure shown in schematic illustration in figures 8, 9 and 12 in which the resonator is supported by a membrane held in isolation from an underlying supporting element, with the actual BAW resonator comprising a first electrode, a piezoelectric layer and a second electrode sandwiched between the first and second electrodes, held above the supporting element and not in contact with the supporting element.

Those having the benefit of the foregoing description of my invention may provide modifications to the embodiment herein described, such as size and shape of the resonator, cavity, vias etc. or may create filters containing more than one resonators adjacent to each other and interconnected electrically. These and other modifications are to be construed as being encompassed within the scope of the present invention as set forth in the appended claims wherein I claim:

Claims

1. A method for fabricating a bulk acoustic resonator on a support wherein the resonator comprises a resonator membrane and wherein the resonator is decoupled from the support by a cavity etched in the support under the resonator, the method comprising using selective etching to etch said cavity through at least one via in said resonator membrane.

2. The method according to claim 1 wherein the selective etching step is selective dry etching.

3. The method according to claim 2 wherein the resonator also comprises a first and a second opposing electrodes on either side of said membrane, the membrane is a piezoelectric layer extending beyond said electrodes over at least a portion of said support and the method further comprises forming a plurality of vias in said piezoelectric membrane adjacent said electrodes prior to using said selective etching to form said cavity and using said selective etching to form said cavity in said support under said first electrode.

4. A method for fabricating a bulk resonator structure on a wafer comprising the steps of:

   (A) forming an isolation layer on an upper surface of said wafer;
   (B) depositing over said isolation layer a first conductive layer and patterning said first conductive layer to form a first electrode;
   (C) depositing over said isolation layer and first electrode a piezoelectric layer;
   (D) forming a second electrode over said piezoelectric layer and over said first electrode;
   (E) opening at least one via through said piezoelectric layer along at least one side of said first electrode and spaced therefrom; and
   (F) forming a cavity under said first electrode and adjacent piezoelectric layer by etching away at least a portion of said isolation layer under said first electrode and adjacent portions of piezoelectric layer, by introducing a selective etchant through said via.

5. The method according to claim 4 wherein said isolation layer is a high resistivity layer.

6. The method according to claim 4 wherein in step (F) the etching process is a dry etching process.

7. The method according to claim 4 wherein in step (F) the cavity extends through said isolation layer into a portion of said wafer.

8. The method according to claim 4 wherein step (E) comprises opening a plurality of vias and wherein said plurality of vias surrounds said first electrode.

9. The method according to claim 4 wherein said wafer is a silicon wafer.

10. The method according to claim 5 wherein said high resistivity layer is deposited by sputtering silicon to form a silicon layer.

11. The method according to claim 10 wherein the step of forming said first electrode comprises using aluminum.

12. The method according to claim 11 wherein the step of forming said piezoelectric layer comprises using AlN.

13. The method according to claim 4 further comprising forming at least one etch delimiting barrier in said wafer and said isolation layer.

14. The method according to claim 13 wherein said wafer is a silicon wafer, said isolation layer is silicon and said etch delimiting barrier is a low temperature oxide.

15. The method according to claim 4 further comprising forming at least one conductive path connected to said second electrode.

16. The method according to claim 15 wherein said conductive path is formed over said piezoelectric layer and connects said second electrode to a wire bonding pad.

17. A bulk acoustic resonator comprising:

(a) a support having a surface;
(b) a cavity extending from the surface of said support into said support;
(c) a piezoelectric membrane extending over said support and said cavity and having an area over said cavity, said membrane having an underside facing said support surface and a topside opposite said underside;
(d) a first electrode adhered to said piezoelectric membrane underside over a portion of said area over said cavity;
(e) a second electrode on said topside of piezoelectric membrane over said first electrode and substantially coextensive with said first electrode;
(f) at least one via in said piezoelectric membrane adjacent said first and second electrodes.

18. The resonator according to claim 17 wherein said support comprises a wafer and an isolation layer in contact with said underside of said piezoelectric membrane.

19. The resonator according to claim 18 wherein said isolation layer is a silicon layer deposited on said wafer.

20. The resonator according to claim 17 comprising a plurality of vias in said piezoelectric membrane and wherein said plurality of vias surrounds said first electrode.

21. The resonator according to claim 18 wherein said wafer is a silicon wafer.

22. The resonator according to claim 17 wherein said first electrode comprises aluminum.

23. The resonator according to claim 17 wherein said piezoelectric layer comprises AlN.

24. The resonator according to claim 17 wherein said support comprises a silicon wafer having a wafer surface, said first and said second electrodes are Al, said piezoelectric membrane is AlN and includes a plurality of vias extending therethrough located adjacent to and around said electrodes, and there is an isolation layer between said membrane undersurface and said wafer surface.

25. The resonator according to claim 24 wherein said vias have a diameter between about $5*10^{-6}$ and about $20*10^{-6}$ meters

26. The resonator according to claim 17 further comprising at least one etch delimiting barrier trench in said isolation layer.

27. The resonator according to claim 26 wherein said support comprises a silicon wafer having a wafer surface, said isolation layer is a silicon layer over said wafer surface and said etch delimiting barrier trench comprises a low temperature oxide.

28. The resonator according to claim 27 further comprising a etch barrier layer extending substantially parallel to said wafer surface in said support under said piezoelectric layer.

29. The resonator according to claim 17 further comprising at least one conductive path extending from said second electrode over said piezoelectric membrane to a wire bonding path outside the membrane area over said cavity.

FIG. 1

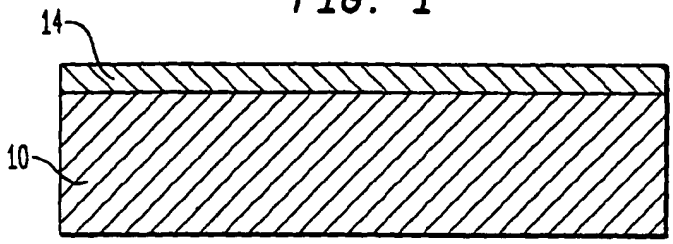


FIG. 2

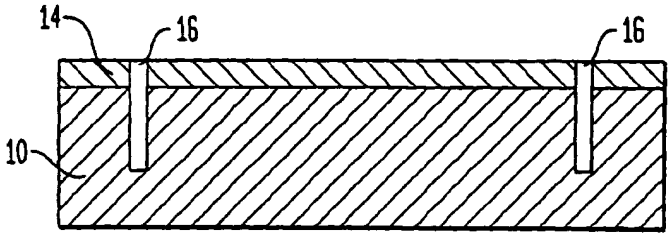


FIG. 3

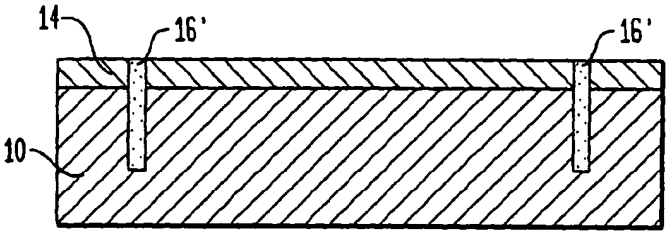


FIG. 4

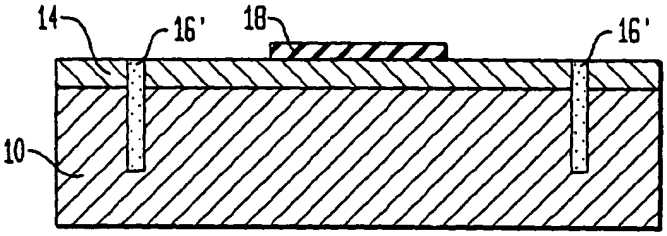


FIG. 5

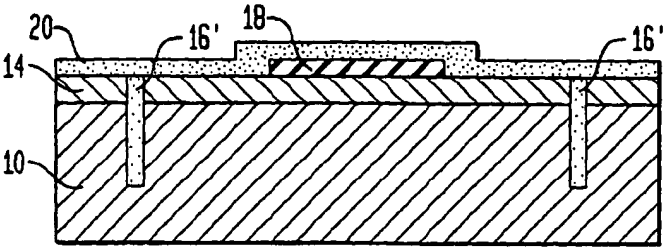


FIG. 6

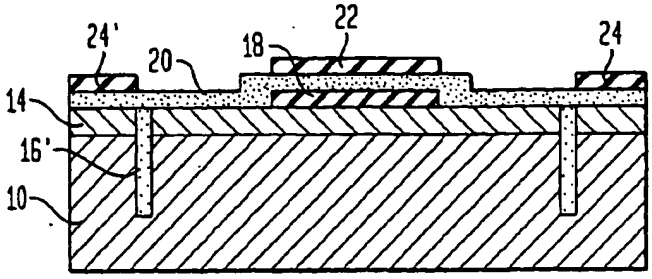


FIG. 7

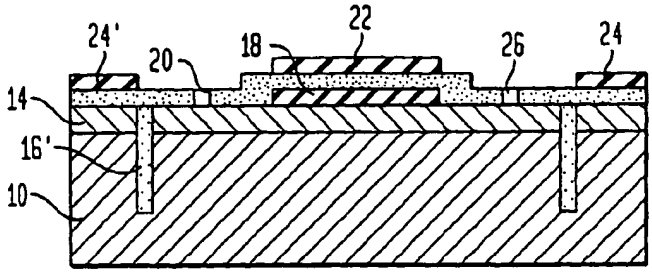


FIG. 8

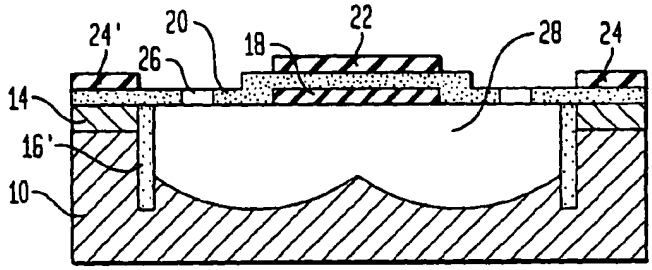


FIG. 9

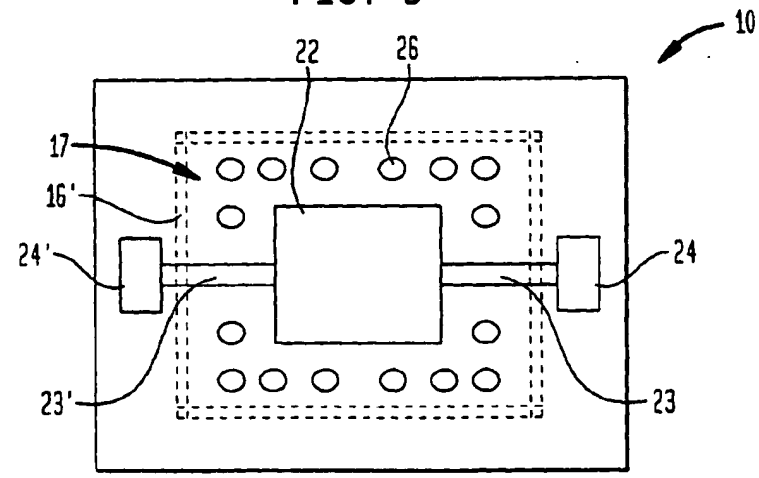


FIG. 10

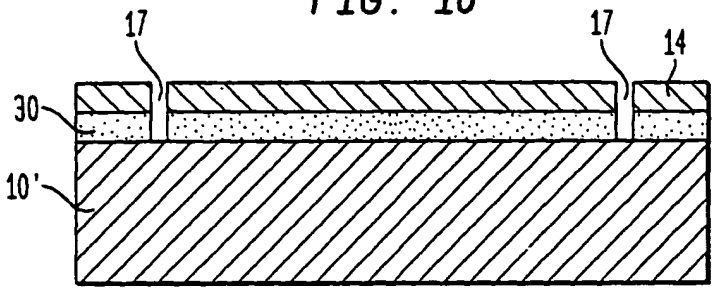


FIG. 11

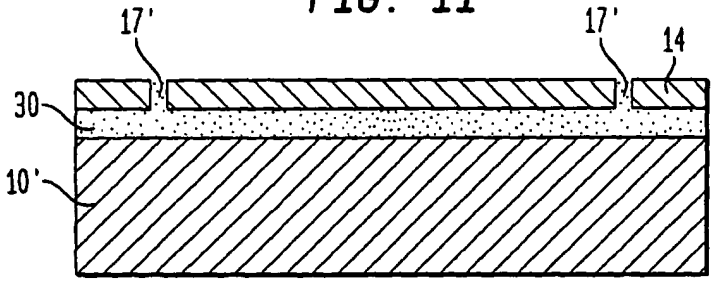


FIG. 12

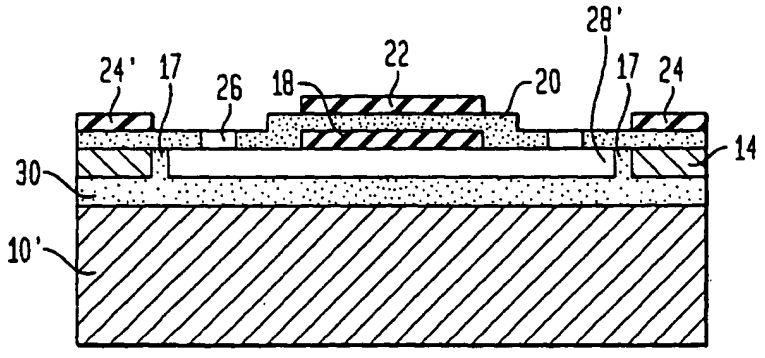


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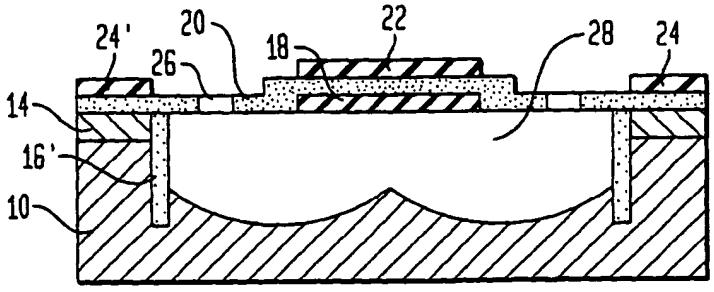
FIG. 8



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EUROPEAN SEARCH REPORT

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 834 989 A (NOKIA MOBILE PHONES LTD) 8 April 1998 (1998-04-08) * figures 2,15-20 * * column 2, line 12 - column 3, line 11 * * column 3, line 22 - line 42 * * column 6, line 57 - column 8, line 31 * * column 11, line 23 - column 13, line 53 * ---	1,4,5, 7-9, 15-18, 20,21, 23,29	B81B3/00 H03H9/17 H03H3/02
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	28 January 2003	Polesello, P

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EUROPEAN SEARCH REPORT

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